CLAIMS:

What is claimed is:

1. A pulse width modulator for a processor having pulse width modulation outputs that are configured to operate based on configuration bits when pulse width modulation outputs are not enabled, comprising:

output control logic;

configuration bits for selectively configuring output control logic; and

an output transistor pair having upper and lower transistors that are respectively coupled to opposing output voltage levels;

the configuration bits causing the output control logic to configure the output pair to operate in one of a tri-state, active high or active low mode when the pair is not enabled for PWM data output.

2. The pulse width modulator according to claim 1, wherein the configuration bits include a tri-state control bit that configures the output pair to operate in one of a tri-state or an active mode.

3. The pulse width modulator according to claim 2, wherein the configuration bits include a high device set bit that configures the output pair to operate in one of an active high or an active low mode when the tri-state control bit configures the output pair to operate in an active mode.

4. The pulse width modulator according to claim 3, wherein the output pair outputs a signal to an external device in an high arrangement.

5. The pulse width modulator according to claim 2, wherein the configuration bits include a high device set bit that configures the output pair to operate in one of an active high or an active low mode when the tri-state control bit configures the output pair to operate in an active mode.

6. The pulse width modulator according to claim 5, wherein the output pair outputs a signal to an external device in an low arrangement.